## AMENDMENTS TO THE CLAIMS

**Claim 1 (original)** A chip scale package of an integrated circuit, comprising:

(a) at least one solder ball pad; and

(b) a moat around each solder ball pad.

**Claim 2 (original)** The chip scale package of claim 1, in which at least one passivation layer is disposed on the integrated circuit, and in which the moat is formed in the at least one passivation layer.

**Claim 3 (original)** The chip scale package of claim 2, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 4 (original)** The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a full-depth moat having a thickness substantially equal to the thickness of the at least one passivation layer.

**Claim 5 (original)** The chip scale package of claim 4, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 6 (original)** The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a partial-depth moat having a thickness of approximately 1-99% of the thickness of the at least one passivation layer.

**Claim 7 (original)** The chip scale package of claim 6, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 8 (original)** The chip scale package of claim 1, in which a first passivation layer is disposed on the integrated circuit, and a second passivation layer, having a thickness, is disposed on the first passivation layer, and in which the moat is formed in the second passivation layer.

**Claim 9 (original)** The chip scale package of claim 8, in which the moat is a full-depth moat having a moat depth substantially equal to the thickness of the second passivation layer.

**Claim 10 (original)** The chip scale package of claim 9, in which at least the second passivation layer comprises a photo-imageable polymer film.

**Claim 11 (original)** The chip scale package of claim 8, in which the moat is a partial-depth moat having a moat depth of approximately 1-99% the thickness of the second passivation layer.

**Claim 12 (original)** The chip scale package of claim 11, in which at least the second passivation layer comprises a photo-imageable polymer film.

**Claim 13 (original)** A wafer for a chip scale package, the wafer having at least one solder ball pad, comprising:

(a) a solder ball at each solder ball pad;

(b) a polymer collar around the solder ball; and

(c) a moat around each solder ball pad.

**Claim 14 (original)** The wafer of claim 13, such that the moat prevents flow of liquefied polymer collar from within the moat to without the moat during and subsequent to heating of the wafer.

**Claims 15-20 (canceled)**

**Claim 21 (new)** The method of claim 1, in which the moat is positioned relative to the solder ball pad to contain liquefied material that may flow to the moat in a direction substantially away from the solder ball pad.

**Claim 22 (new)** The method of claim 2, in which the at least one passivation layer is an insulating layer.

**Claim 23 (new)** The method of claim 13, in which the moat is positioned relative to the solder ball pad to contain liquefied material that may flow to the moat in a direction substantially away from the solder ball pad.

**Claim 24 (new)** The method of claim 13, in which at least a portion of the polymer collar is positioned at a height, relative to the wafer, above the top of the moat.

**Claim 25 (new)** The method of claim 13, in which the moat is formed in a passivation layer.

**Claim 26 (new)** The method of claim 13, in which the moat is formed in an insulating layer.